OIPE JC21
DEC 0 6 2004
PATENT & TRADEMARK OFFICE

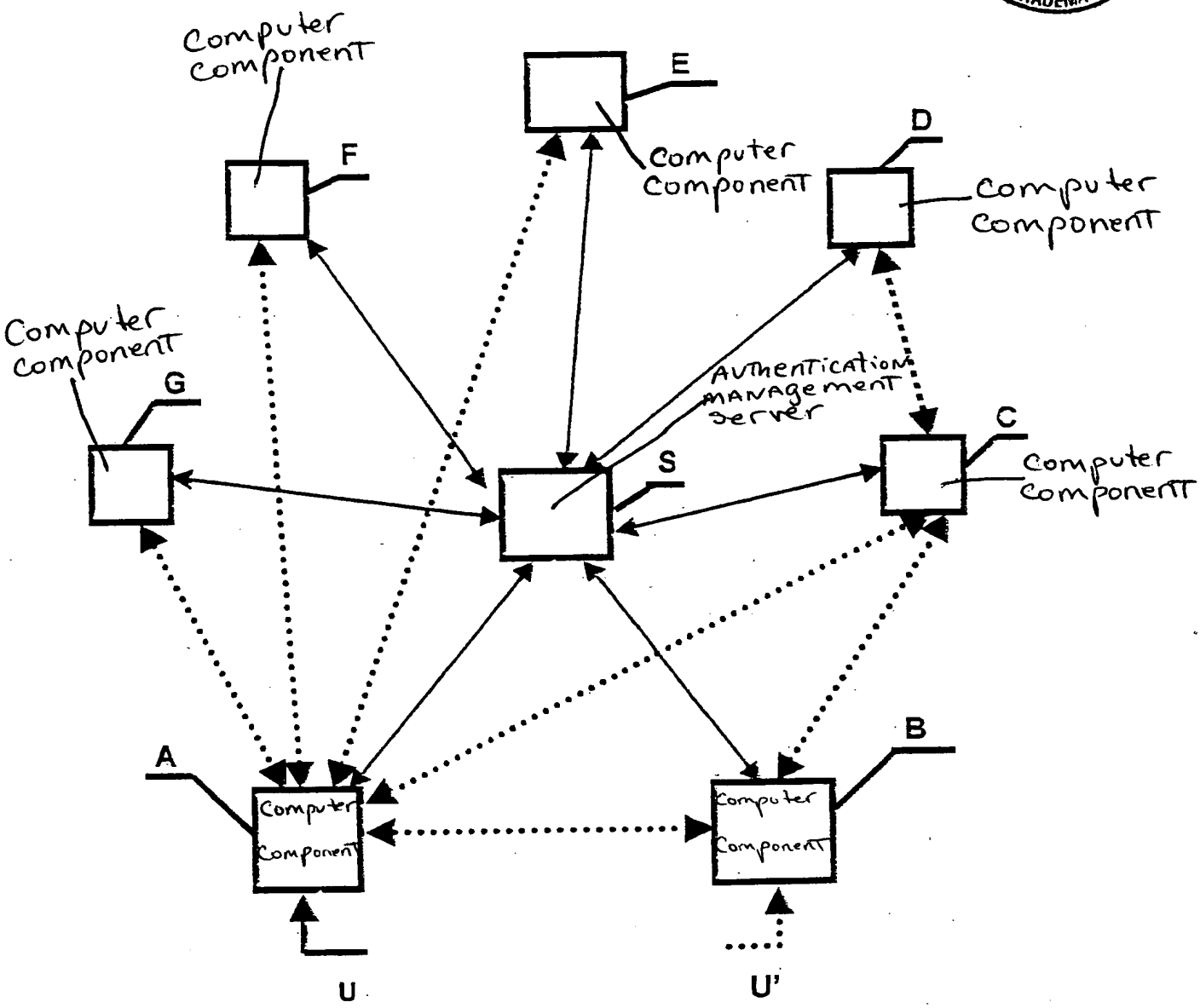

FIG.1

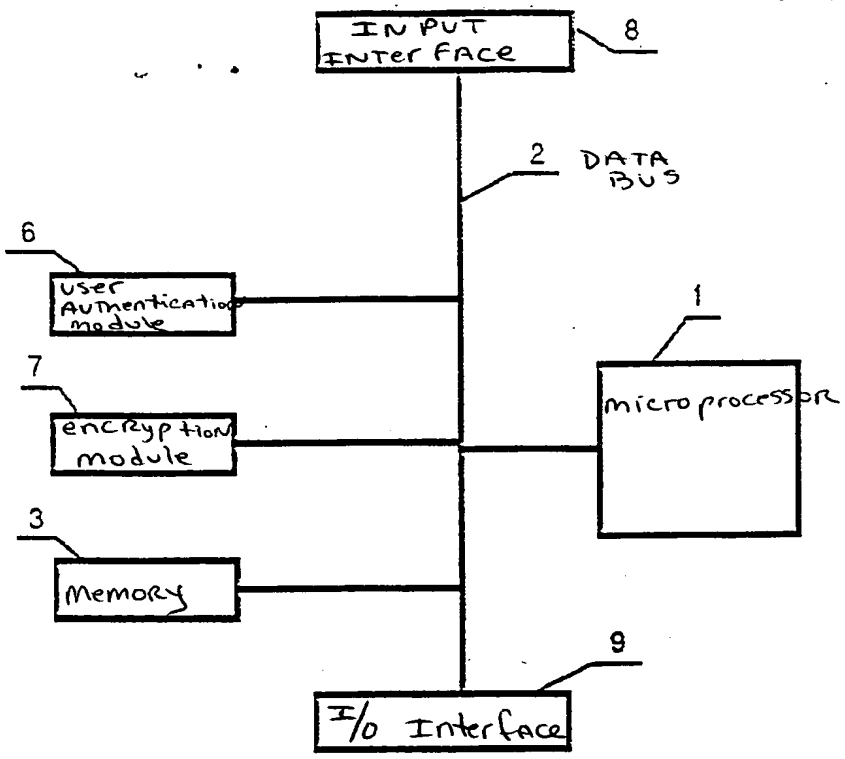
INPUT INTERFACE
8
2 DATA BUS
6
USER AUTHENTICATION MODULE
1
MICROPROCESSOR
7
ENCRYPTION MODULE
3
MEMORY
9
I/O INTERFACE

FIG. 2

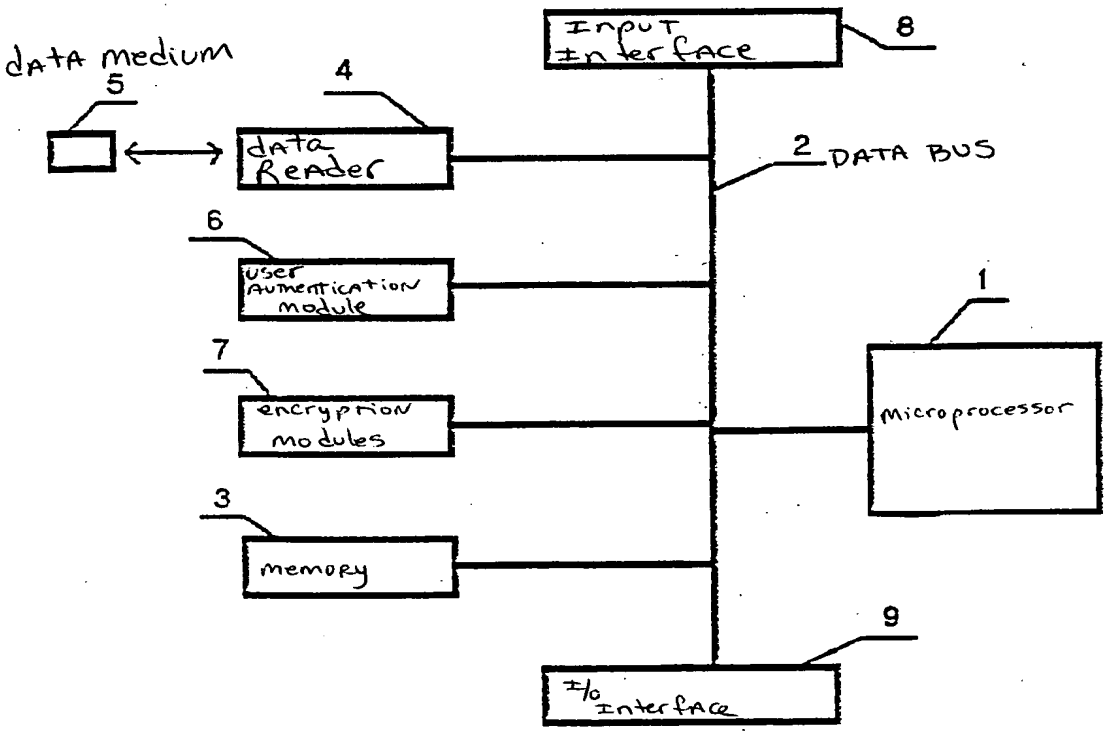
DATA MEDIUM
5
4
INPUT INTERFACE
8
DATA READER
2 DATA BUS
6
USER AUTHENTICATION MODULE
1
MICROPROCESSOR
7
ENCRYPTION MODULES
3
MEMORY
9
I/O INTERFACE

FIG. 3

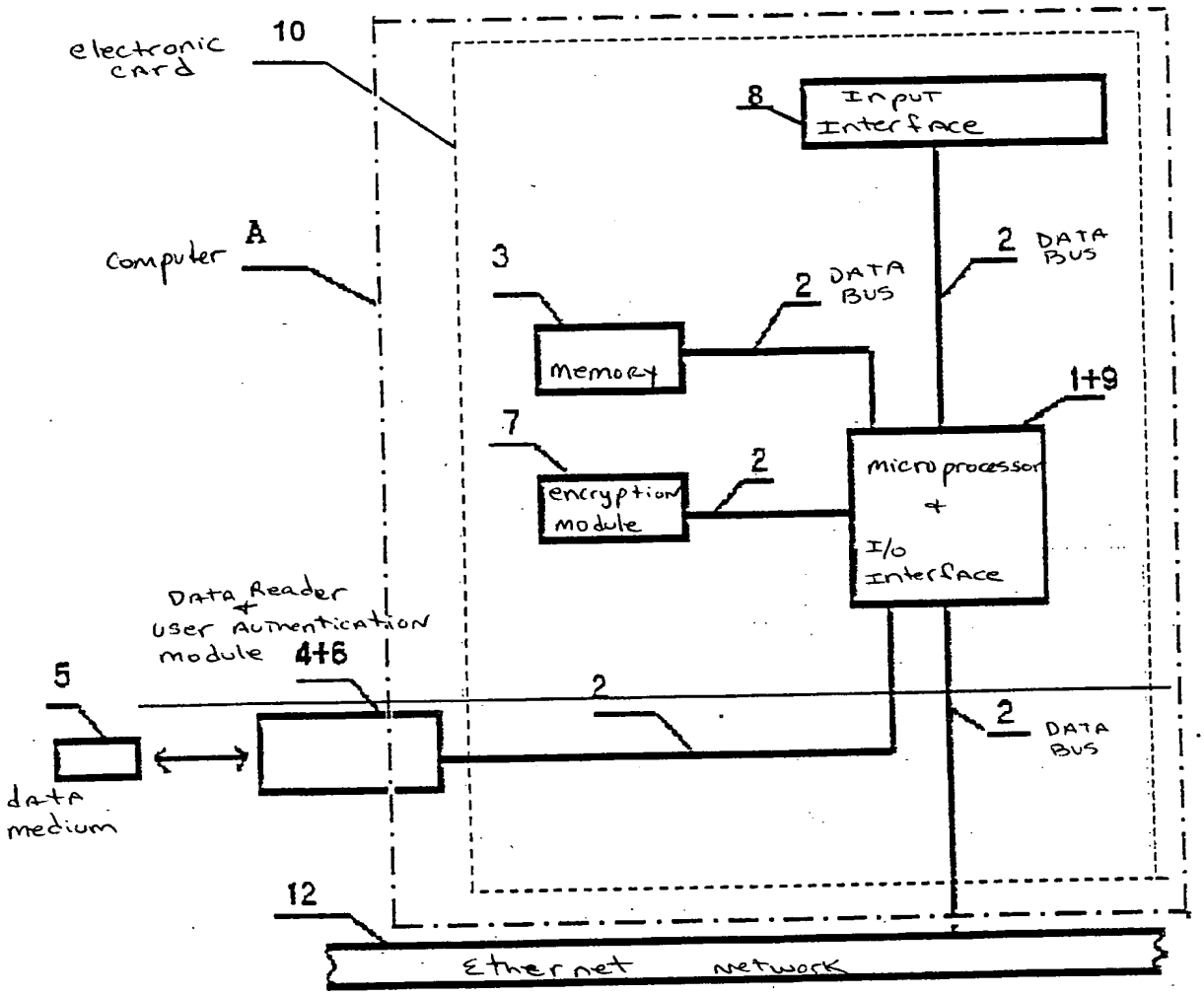
electronic card
10
8
Input Interface
Computer
A
3
2 DATA BUS
2 DATA BUS
Memory
1+9
7
2
encryption module
micro processor + I/O Interface
Data Reader + User Authentication module
4+6
5
2
2 DATA BUS
data medium
12
Ethernet network

FIG. 4

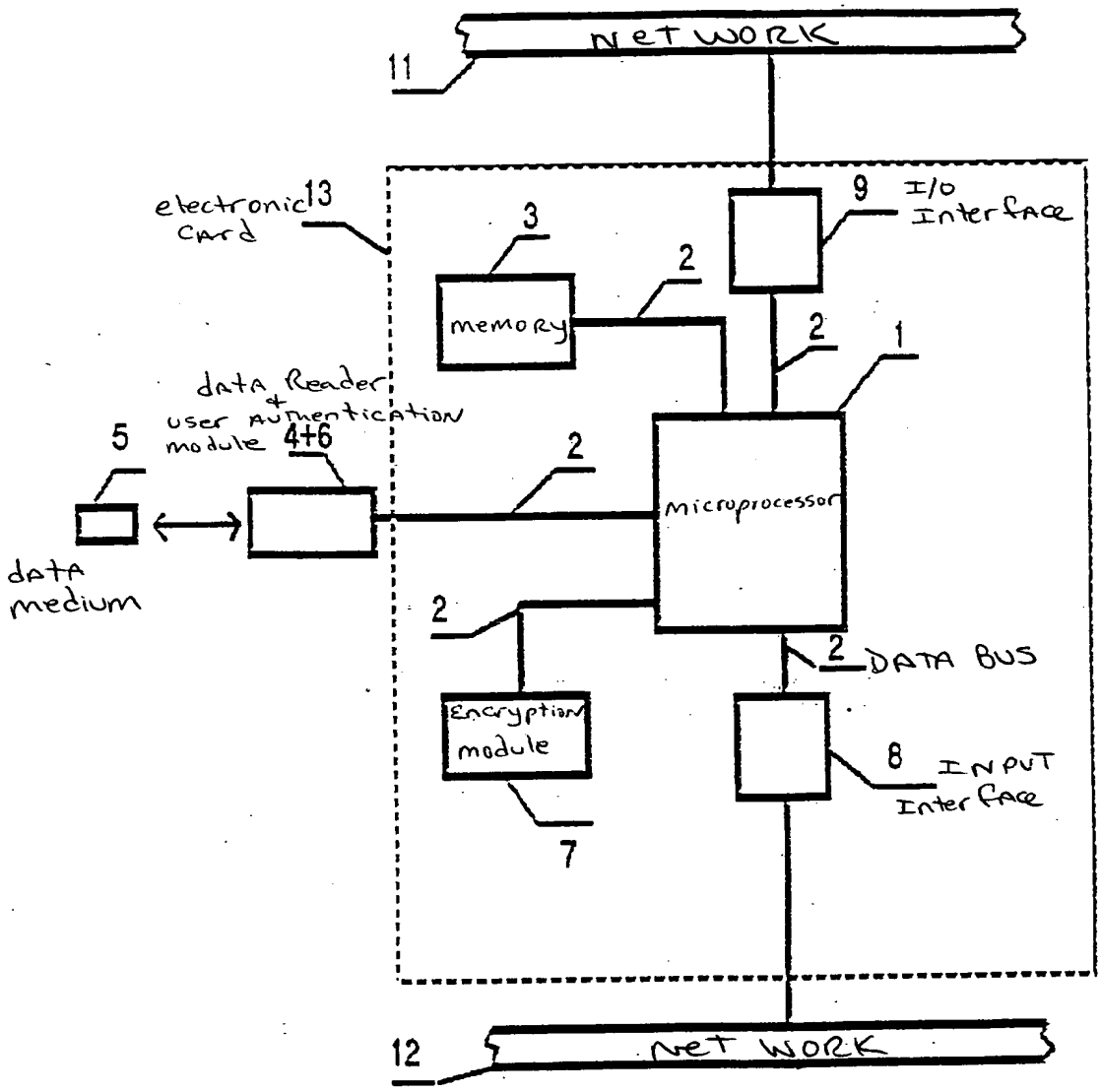
NETWORK
11
electronic card
13
9 I/O Interface
3
memory
2
2
1
data Reader & user authentication module
4+6
5
2
microprocessor
data medium
2
2 DATA BUS
Encryption module
7
8 INPUT Interface
12
NET WORK

FIG. 5

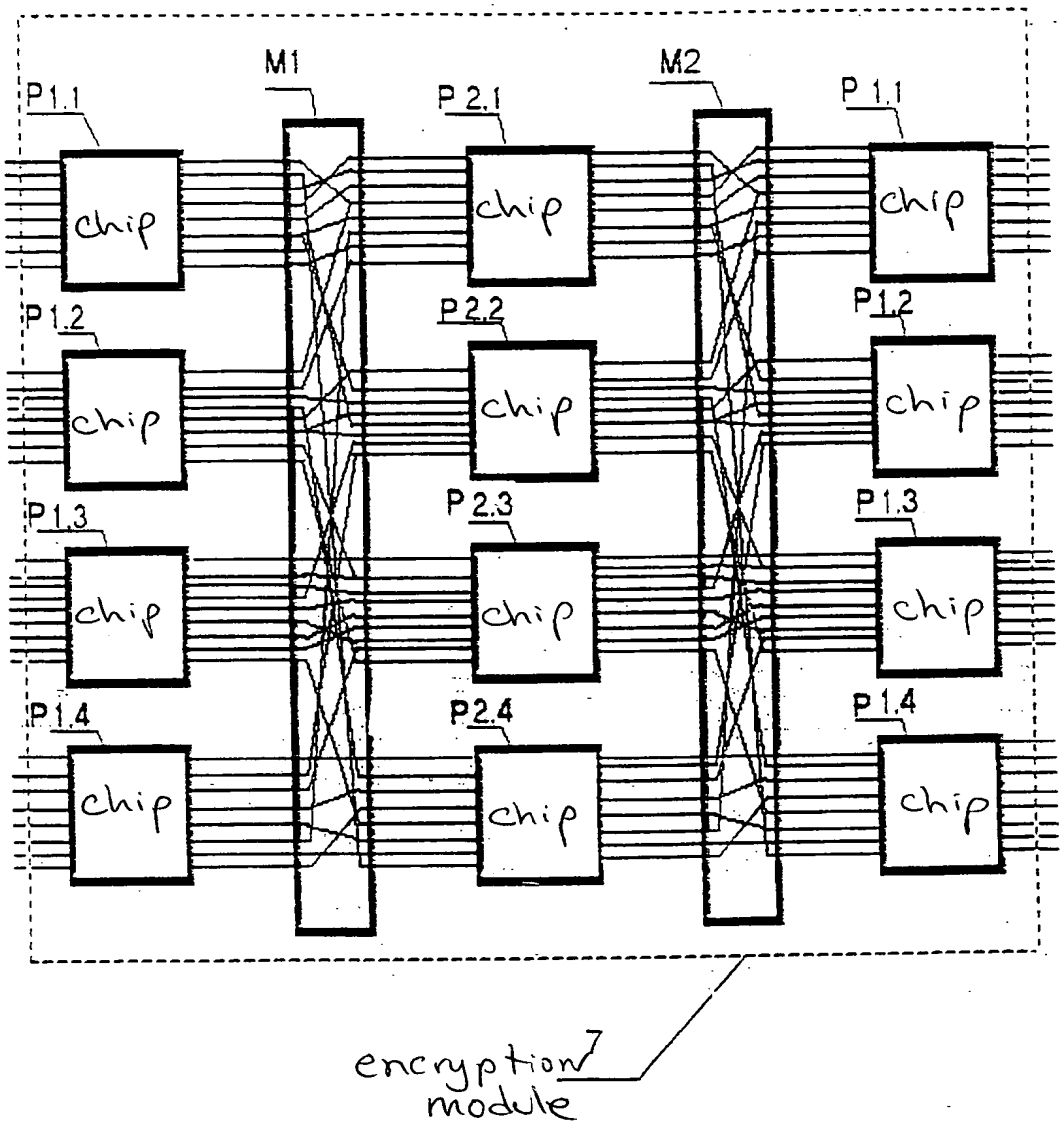
M1
M2
P1.1
P2.1
P1.1
P1.2
P2.2
P1.2
P1.3
P2.3
P1.3
P1.4
P2.4
P1.4
chip
encryption module

FIG. 6

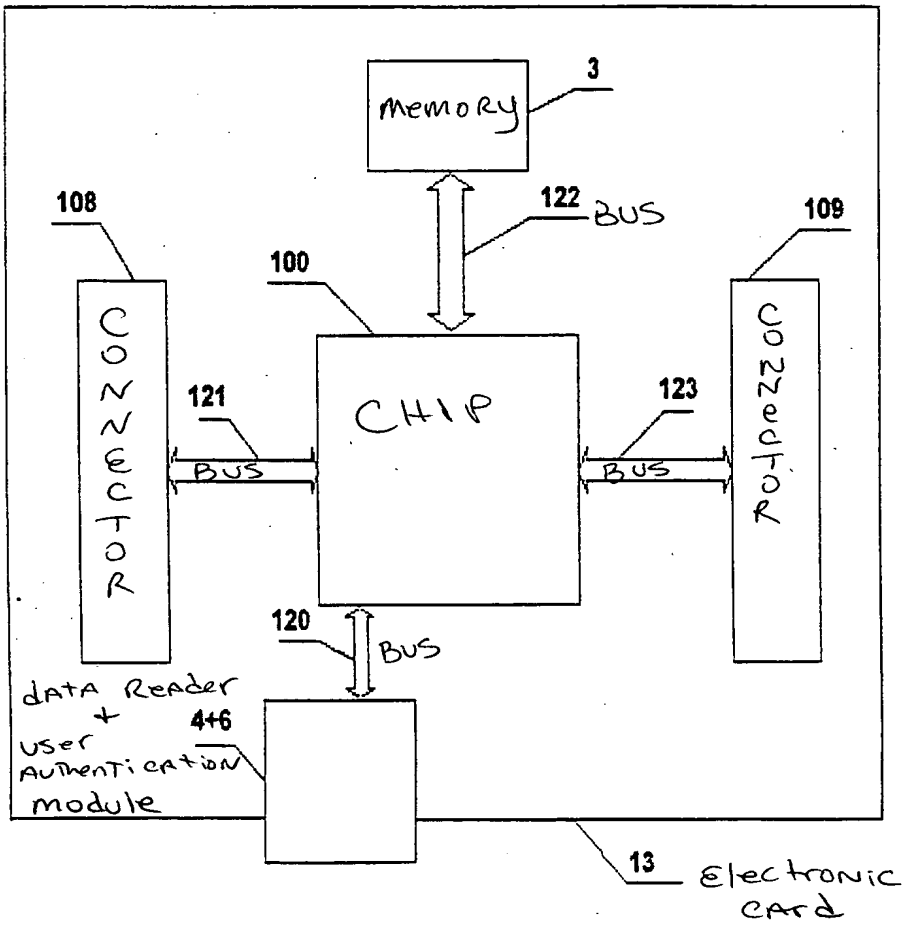
memory
3
122 BUS
108
109
100
CONNECTOR
CHIP
connector
121
123
BUS
BUS
120
BUS
data Reader
+
user
authentication
module
4+6
13
electronic
card

FIG. 7

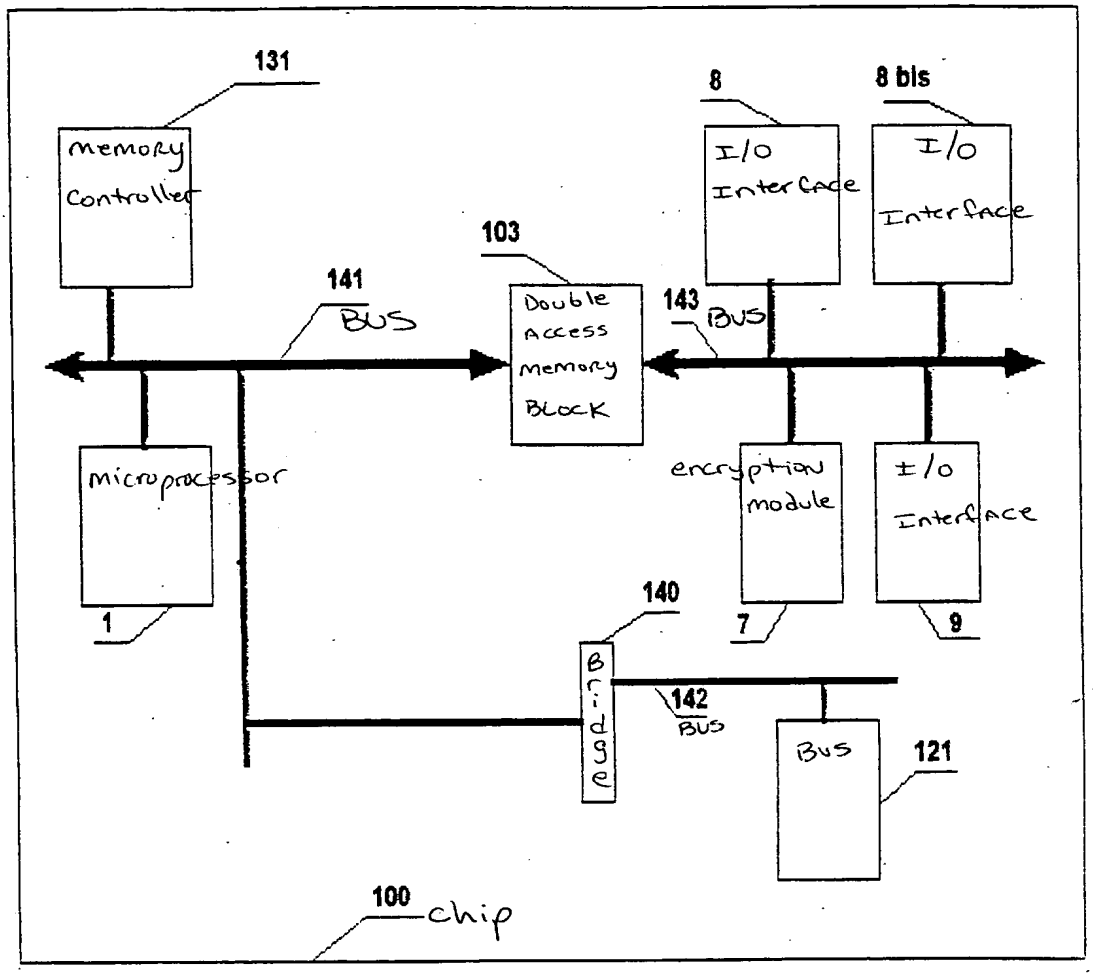
131
memory Controller
8
I/O Interface
8 bis
I/O Interface
103
Double Access Memory Block
141 BUS
143 BUS
microprocessor
1
encryption module
7
I/O Interface
9
140
Bridge
142 BUS
Bus
121
100 chip

FIG.8